REVISIONS

	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add package outline 3. Editorial changes throughout.	95-03-29	T. Hess

REV																				
SHEET																				
REV	A	A																		
SHEET	15	16																		

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
19 September 1990

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, ASYNCHRONOUS, SERIAL CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89725
A	67268	

SHEET 1 OF 16

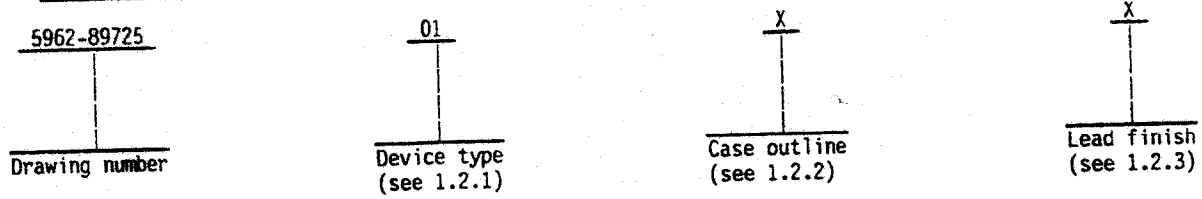
DESC FORM 193
JUL 94

5962-E155-95

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82510	CHMOS single component asynchronous serial controller 1/
02	82510	CHMOS single component asynchronous serial controller 2/

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
3	CQCC1-N28	28	square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Voltage on any pin with respect to GND	-0.5 V dc to V_{CC} + 0.5
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 3/	250 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction Temperature (T_J)	150°C
Lead temperature (soldering, 10 seconds)	265°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ V_{IH} = 2.4 V min.
2/ V_{IH} = 2.6 V min.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage	V_{IL}		1, 2, 3	1/ -0.5	0.8	V
Input high voltage	V_{IH}			2/	1/ V_{CC} +0.5	
Output low voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	
Output high voltage	V_{OH}	I_{OH} = -0.4 mA		2.4		
Input leakage current	I_{IL1}	$0.0\ V\ dc \le V_{IN} \le V_{CC}$			±10	µA
Three-state leakage current	I_{IL2}	$0.45\ V\ dc \le V_{OUT} \le V_{CC} - 0.45\ V$			±10	
Power supply current	I_{CC}	V_{CC} = 5.5 V, V_{IL} = 0.5 V, $V_{IH} \ge V_{CC} - 0.5$ V, $I_{OL} = I_{OH}$ = 0.0, EXT 1 x CLK			3.8	mA/ MHz
Standby supply current	I_{STBY}	V_{CC} = 5.5 V, $V_{IL} \le 0.5$ V, $V_{IH} \ge V_{CC} - 0.5$ V, $I_{OL} = I_{OH}$ = 0.0 V			500	µA
$\overline{RTS}$, $\overline{DTR}$, strapping current	I_{OHR}				0.4	mA
	I_{OLR}			11		
Input capacitance	C_{IN}	Frequency = 1 MHz See 4.3.1c 1/	4		10	pF
I/O capacitance	C_{IO}				10	
X1, X2 load	C_{XTAL}	1/	1, 2, 3		10	
Functional tests		See 4.3.1d	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
CLK period 3/	$t_{CY/2}$	See figure 3	9, 10, 11	54	250	ns
CLK low time 3/	t_{CLCH}			25		
CLK high time 3/	t_{CHCL}			25		
CLK rise time 1/ 3/ 4/	t_{CH1CH2}				10	
CLK fall time 1/ 3/ 5/	t_{CL2CL1}				10	
External crystal frequency rating 1/ 3/	f_{XTAL}			4.0	18.43	MHz
CLK period 6/	t_{CY}			108		ns
CLK low time 6/	t_{CLCH}			54		
CLK high time 6/	t_{CHCL}			44	250	
CLK rise time 1/ 4/ 6/	t_{CH1CH2}				15	
CLK fall time 1/ 5/ 6/	t_{CL2CL1}				15	
RESET width - CLK/X1 configured to CLK	t_{RSHL}	See figure 3, reset timing		$8t_{CY}$		
$\overline{RTS}/\overline{DTR}$ low setup to RESET inactive	t_{TLRSL}			$6t_{CY}$		
$\overline{RTS}/\overline{DTR}$ low hold after RESET inactive 1/	t_{RSLTX}			0	t_{CY}-20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{RD}$ active width	t_{RLRH}	See figure 3, read cycle timing	9, 10, 11	$2t_{CY}+65$		ns
Address/$\overline{CS}$ setup time to $\overline{RD}$ active	t_{AVRL}			7		
Address/$\overline{CS}$ hold time after $\overline{RD}$ inactive	t_{RHAX}			0		
Data out valid delay after $\overline{RD}$ active	t_{RLDV}			$2t_{CY}+65$		
Command inactive to active delay	t_{CIAD}			$t_{CY}+15$		
Data out float delay after $\overline{RD}$ inactive	t_{RHDZ}				40	
$\overline{WR}$ active width	t_{WLWH}	See figure 3, write cycle timing		$2t_{CY}+15$		
Address $\overline{CS}$ setup time to $\overline{WR}$ active	t_{AVWL}			7		
Address and $\overline{CS}$ hold time after $\overline{WR}$	t_{WHAX}			0		
Data in setup time to $\overline{WR}$ inactive	t_{DVWH}			90		
Data in hold time after $\overline{WR}$ inactive	t_{WHDX}			12		
SCLK period 7/	t_{XCY}	See figure 3, setup and hold times waveforms		216		
SCLK low time 1/ 7/	t_{XLXH}			93		
SCLK high time 1/ 7/	t_{XHXL}			93		
SCLK rise time 1/ 4/ 7/	t_{XH1XH2}				15	
SCLK fall time 1/ 5/ 7/	t_{XL2XL1}				15	
SCLK period 8/	t_{XCY}			3500		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
SCLK low time 1/ 8/	t_{XLXH}	See figure 3, setup and hold times waveforms	9, 10, 11	1650		ns
SCLK high time 1/ 8/	t_{XHXL}			1650		
SCLK rise time 1/ 4/ 8/	t_{XH1XH2}				15	
SCLK fall time 1/ 5/ 8/	t_{XL2XL1}				15	
RXD setup time to SCLK high 8/	t_{RPW}			250		
RXD hold time after SCLK high 8/	t_{RPD}			250		
TXD valid delay after SCLK low 8/	$t_{SCLKTXD}$				170	
TXD delay after RXD	t_{RXDTXD}				170	

1/ Guaranteed to the limits specified, if not tested.
2/ The minimum input voltage high for device 01 V_{IH} = 2.4, for device 02 V_{IH} = 2.6.
3/ Divide by two option active.
4/ From 0.8 V dc to 2.0 V dc.
5/ From 2.0 V dc to 0.8 V dc.
6/ Divide by two option inactive.
7/ SCLK pin specification 16x clocking mode.
8/ SCLK pin specification 1x clocking mode.

Case X, 3

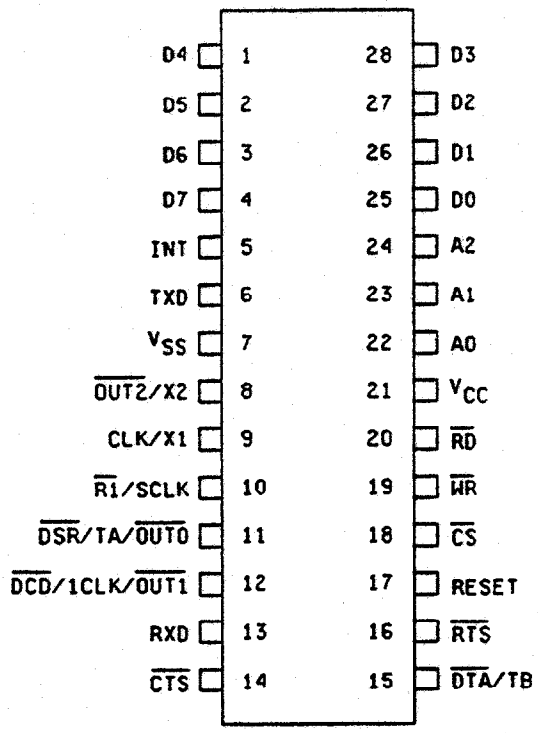


Figure 1. Terminal Connections.

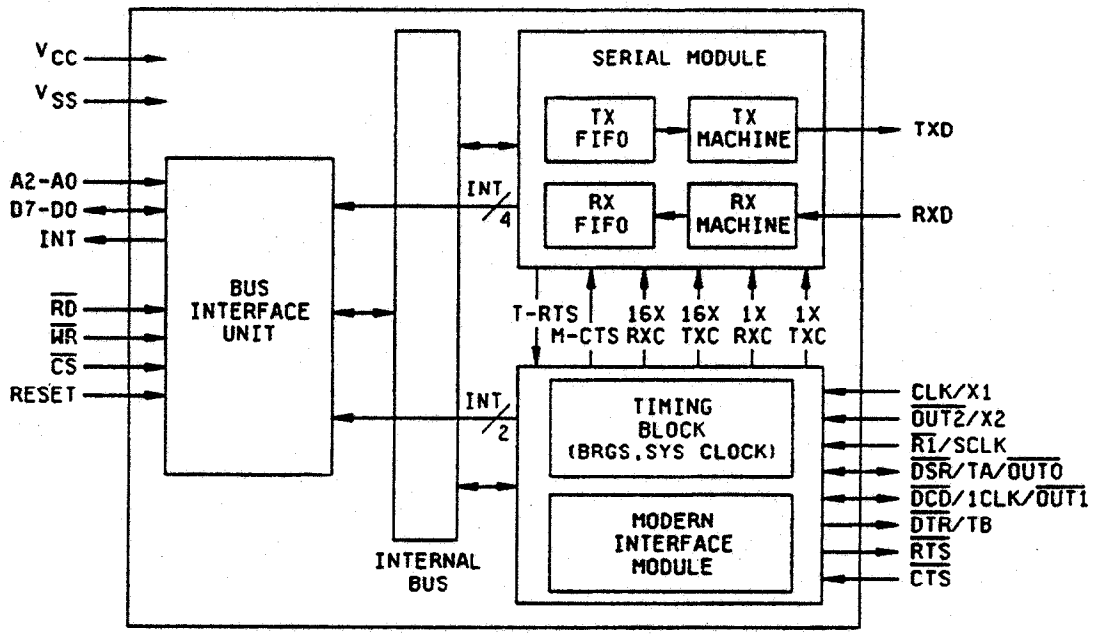
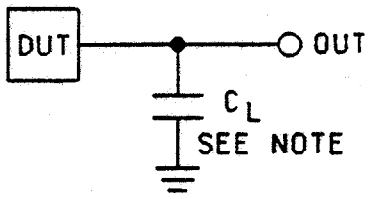
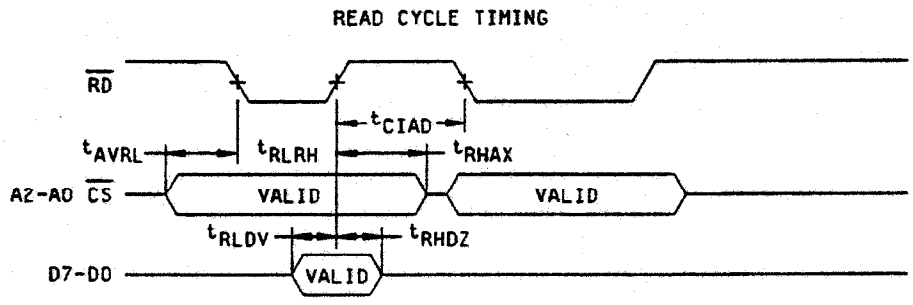


Figure 2. Functional block diagram.



Note: C_L = 20 to 100 pF

Read cycle timing



Note: AC testing inputs are driven at 2.4 V for logic 1 and 0.45 V for logic 0. Timing measurements are made at 1.5 V for both a logic 1 and 0.

Figure 3. Test circuit and switching waveforms.

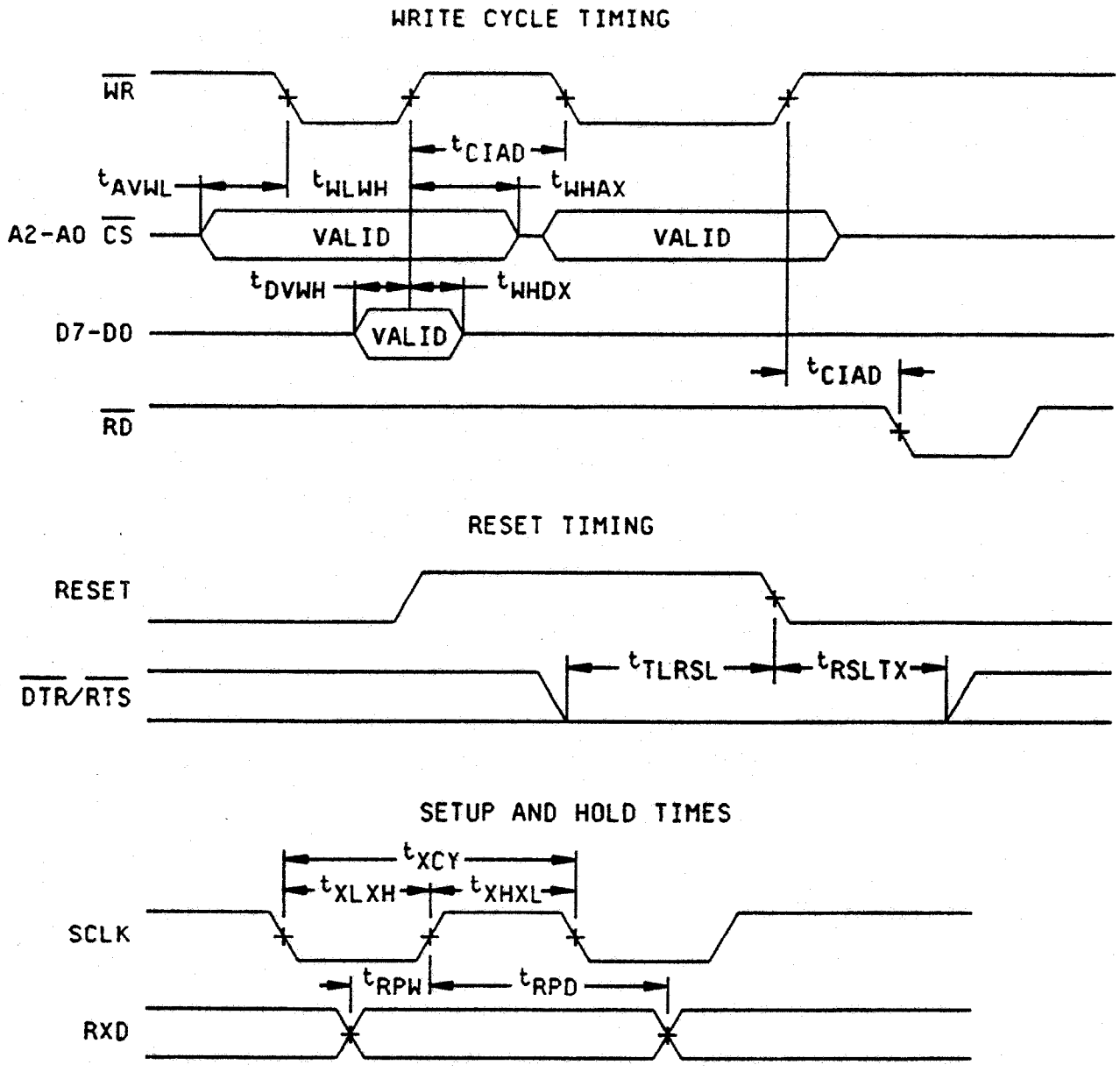


Figure 3. Test circuit and switching waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required

d. Subgroups 7 and 8 shall include verification of the funtionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Pin descriptions.

Pin	Type	Description
RESET	I	A high on this input pin resets device 01 to the default wake-up mode.
$\overline{CS}$	I	A low on this input pin enables device 01 and allows read or write operations.
A2-A0	I	These inputs interface with three bits of the system address bus to select one of the internal registers for read or write.
D7-D0	I/O	Bi-directional, three state, 8-bit data bus. These pins allow transfer of bytes between the CPU and device 01.
$\overline{RD}$	I	A low on this input pin allows the CPU to read data or status bytes from device 01.
$\overline{WR}$	I	A low on this input allows the CPU to write data or control bytes to device 01.
INT	O	A high on this output pin signals an interrupt request to the CPU. The CPU may determine the particular source and cause of the interrupt by reading device 01's status registers.
CLK/X1	I	This input pin serves as a source for the internal system clock. The clock may be asynchronous to the serial clocks and to the processor clock. This pin may be used in one of two modes: CLK - in this mode an externally generated TTL compatible clock should be used to drive this input pin; X1 - in this mode the clock is internally generated by an on-chip crystal oscillator. This mode requires a crystal to be connected between this pin (X1) and the X2 pin.
$\overline{OUT2}$/X2	O	This is a dual function pin which may be configured to one of the following functions: $\overline{OUT2}$ - a general purpose output pin controlled by the CPU, only available when CLK/X1 pin is driven by an externally generated clock; X2 - this pin serves as an output pin for the crystal oscillator. The configuration of the pin is done only during hardware reset.
TXD	O	Serial data is transmitted via this output pin starting at the least significant bit.
RXD	I	Serial data is received on this input pin starting at the least significant bit.

6.5 Pin descriptions - Continued.

Pin	Type	Description
$\overline{RI}$/SCLK	I	This is a dual function pin which can be configured to one of the following functions: $\overline{RI}$ - ring indicator - input, active low. This is a general purpose input pin accessible by the CPU. SCLK - this input pin may serve as a source for the internal serial clock(s), RxClk and/or TxClk.
$\overline{DTR}$/TB	O	This is a dual function pin which may be configured to one of the following functions. $\overline{DTR}$ - data terminal ready, output, active low. This is a general purpose output pin controlled by the CPU. TB - this pin outputs the BRGB output signal when configured as either a clock generator or as a timer. When BRGB is configured as a timer this pin outputs a "timer expired pulse". When BRGB is configured as a clock generator it outputs the BRGB output clock.
$\overline{DSR}$/TA/$\overline{OUT0}$	I/O	This is a multifunction pin which may be configured to one of the following functions. $\overline{DSR}$ - data set ready, input, active low. This is a general purpose input pin accessible by the CPU. TA - this pin is similar in function to pin TB except it outputs the signal from BRGA instead of BRGB. $\overline{OUT0}$ - output pin. This is a general purpose output pin controlled by the CPU.
$\overline{RTS}$	O	Request to send: Output pin, active low. This is a general purpose output pin controlled by the CPU. In addition, in automatic transmission mode this pin, along with $\overline{CTS}$, controls the transmission of data. During hardware reset this pin is an input. It is used to determine the system clock mode.
$\overline{CTS}$	I	Clear to send: Input pin, active low. In automatic transmission mode it directly controls the transmit machine. This pin can be used as a general purpose input.
$\overline{DCD}$/ICLK/$\overline{OUT1}$	I/O	Multifunction: This is a multifunction pin which may be configured to one of the following functions. $\overline{DCD}$ - data carrier detected, input pin, active low. This is a general purpose input pin accessible by the CPU. ICLK - this pin is the output of the internal system clock. $\overline{OUT1}$ - general purpose output pin, controlled by the CPU.
V_{SS}	P	Ground.
V_{CC}	P	Power: + 5 V supply.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-03-29

Approved sources of supply for SMD 5962-89725 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8972501XX	34649	MD82510/B
5962-89725023X	34649	MR82510/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation Robert Noyce Building FS001 2200 Mission College Blvd. P.O. Box 58119 Santa Clara, CA 95052-8119 Point of contact: 5000 West Chandler Blvd Chandler, AZ 85226